The SP8690 and SP8691 are low power ECL variable modulus dividers, with both ECL10K and TTL/CMOS compatible outputs. They divide by the lower division ratio when either of the ECL control inputs, PE1 or PE2, is in the high state and by the higher ratio when both are low (or open circuit).

**FEATURES**
- ECL and TTL/CMOS Compatible Outputs
- AC-Coupled Input
- Control Inputs ECL Compatible

**QUICK REFERENCE DATA**
- Supply Voltage: −5.2V±0.25V (ECL), 5V±0.25V (TTL)
- Power Consumption: 70mW (Typ.)
- Temperature Range:
  - −55°C to +125°C (A Grade)
  - −30°C to +70°C (B Grade)

**ABSOLUTE MAXIMUM RATINGS**
- Supply voltage, $|V_{CC} - V_{EE}|$: 8V
- ECL output current: 10mA
- Storage temperature range: −65°C to +150°C
- Max. junction temperature: +175°C
- TTL output voltage: +12V
- Input voltage: 2.5V p-p
- Max. open collector current: 15mA

**ORDERING INFORMATION**
- SP8690 A DG
- SP8690 B DG
- SP8691 A DG
- 5962-87678 (SMD) (SP8690)
ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range.

ECL OPERATION

Supply voltage, \( V_{CC} = 0V, \ V_{EE} = -5.2V \pm 0.25V \)
Temperature, \( T_{AMB} = -55^\circ C \) to \(+125^\circ C \) (A Grade), \(-30^\circ C \) to \(+70^\circ C \) (B Grade)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
<th>Conditions</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum frequency (sinewave input)</td>
<td>( f_{MAX} )</td>
<td>200</td>
<td>MHz</td>
<td>Input = 400-800mV p-p</td>
<td>5</td>
</tr>
<tr>
<td>Minimum frequency (sinewave input)</td>
<td>( f_{MIN} )</td>
<td>40</td>
<td>MHz</td>
<td>Input = 400-800mV p-p</td>
<td>5</td>
</tr>
<tr>
<td>Power supply current</td>
<td>( I_{EE} )</td>
<td>21</td>
<td>mA</td>
<td>( V_{EE} = -5.0V )</td>
<td>5</td>
</tr>
<tr>
<td>ECL output high voltage</td>
<td>( V_{OH} )</td>
<td>-0.85</td>
<td>V</td>
<td>( V_{EE} = -5.2V ) (25°C)</td>
<td>5</td>
</tr>
<tr>
<td>ECL output low voltage</td>
<td>( V_{OL} )</td>
<td>-1.5</td>
<td>V</td>
<td>( V_{EE} = -5.2V ) (25°C)</td>
<td>5</td>
</tr>
<tr>
<td>PE input high voltage</td>
<td>( V_{INH} )</td>
<td>-0.93</td>
<td>V</td>
<td>( V_{EE} = -5.2V ) (25°C)</td>
<td>5</td>
</tr>
<tr>
<td>PE input low voltage</td>
<td>( V_{INL} )</td>
<td>-1.62</td>
<td>V</td>
<td>( V_{EE} = -5.2V ) (25°C)</td>
<td>5</td>
</tr>
<tr>
<td>Clock to ECL output delay</td>
<td>( t_{PLH} )</td>
<td>9</td>
<td>ns</td>
<td></td>
<td>6</td>
</tr>
<tr>
<td>Set-up time</td>
<td>( t_{S} )</td>
<td>3</td>
<td>ns</td>
<td></td>
<td>3, 6</td>
</tr>
<tr>
<td>Release time</td>
<td>( t_{r} )</td>
<td>8</td>
<td>ns</td>
<td></td>
<td>3, 6</td>
</tr>
</tbody>
</table>

TTL OPERATION

Supply voltage, \( V_{CC} = 5V \pm 0.25V, \ V_{EE} = 0V \)
Temperature, \( T_{AMB} = -55^\circ C \) to \(+125^\circ C \) (A Grade), \(-30^\circ C \) to \(+70^\circ C \) (B Grade)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
<th>Conditions</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum frequency (sinewave input)</td>
<td>( f_{MAX} )</td>
<td>200</td>
<td>MHz</td>
<td>Input = 400-800mV p-p</td>
<td>5</td>
</tr>
<tr>
<td>Minimum frequency (sinewave input)</td>
<td>( f_{MIN} )</td>
<td>40</td>
<td>MHz</td>
<td>Input = 400-800mV p-p</td>
<td>5</td>
</tr>
<tr>
<td>Power supply current</td>
<td>( I_{EE} )</td>
<td>21</td>
<td>mA</td>
<td>( V_{CC} = 5.0V )</td>
<td>5</td>
</tr>
<tr>
<td>TTL output low voltage</td>
<td>( V_{OL} )</td>
<td>0.5</td>
<td>V</td>
<td>( V_{CC} = 5V, R_{L} = 560\Omega )</td>
<td>5, 7</td>
</tr>
<tr>
<td>TTL output high voltage</td>
<td>( V_{OH} )</td>
<td>3.75</td>
<td>V</td>
<td>( V_{CC} = 5V, R_{L} = 560\Omega )</td>
<td>5, 7</td>
</tr>
<tr>
<td>Clock to TTL output high delay, +ve going</td>
<td>( t_{PLH} )</td>
<td>32</td>
<td>ns</td>
<td>( R_{L} = 560\Omega )</td>
<td>6</td>
</tr>
<tr>
<td>Clock to TTL output low delay, -ve going</td>
<td>( t_{PFL} )</td>
<td>18</td>
<td>ns</td>
<td>( R_{L} = 560\Omega )</td>
<td>6</td>
</tr>
<tr>
<td>Set-up time</td>
<td>( t_{S} )</td>
<td>3</td>
<td>ns</td>
<td></td>
<td>3, 6</td>
</tr>
<tr>
<td>Release time</td>
<td>( t_{r} )</td>
<td>8</td>
<td>ns</td>
<td></td>
<td>3, 6</td>
</tr>
</tbody>
</table>

NOTES

1. The temperature coefficients of \( V_{OH} = +1.63mV/\degree C, \ V_{OL} = +0.94mV/\degree C \) and of \( V_{IN} = +1.22mV/\degree C \).
2. The test configuration for dynamic testing is shown in Fig.8.
3. The set-up time \( t_{S} \) is defined as the minimum time that can elapse between \( L \rightarrow H \) transition of control input and the next \( L \rightarrow H \) clock pulse transition to ensure that division by the lower modulus is obtained.
4. The release time \( t_{r} \) is defined as the minimum time that can elapse between \( H \rightarrow L \) transition of control input and the next \( L \rightarrow H \) clock pulse transition to ensure that division by the higher modulus is obtained.
5. SP8690/1B tested at 25°C only.
6. Guaranteed but not tested.
7. The open collector output is not recommended for use at output frequencies above 15MHz. \( C_{LOAD} \leq 5pF \).
**Truth Table for Control Inputs**

<table>
<thead>
<tr>
<th>PE1</th>
<th>PE2</th>
<th>Division ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>11</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>10</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>10</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>10</td>
</tr>
</tbody>
</table>

**Fig. 4 Timing diagram, SP8690**

**Fig. 5 Timing diagram, SP8691**

**Fig. 6 Typical input characteristics, SP8690/1**

**Fig. 7 Typical input impedance. Test conditions: Supply Voltage = 5.0V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.**
Fig. 8 Test circuit for dynamic measurements

Fig. 9 Typical application showing interfacing.

OPERATING NOTES

1. The clock inputs can be single or differentially driven. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to ground.

2. In the absence of a signal the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 68kΩ resistor from the input to VEE, i.e., from pin 1 or pin 16 to pin 12. This reduces the input sensitivity by approximately 100mV.

3. The circuit will operate down to DC but slew rate must be better than 100V/μs.

4. The Q4 and Q5 outputs are compatible with ECLII but can be interfaced to ECL10K as shown in Fig. 9.

5. The PE inputs are ECLIII/10K compatible and include internal 10kΩ pulldown resistors. Unused inputs can therefore be left open circuit.

6. The input impedance of the SP8690/1 varies as a function of frequency. See Fig. 7.

7. The TTL/CMOS output is a free collector and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed 12V.

8. The rise/fall time of the open collector output waveform is directly proportional to load capacitance and load resistor value. Therefore, load capacitance should be minimised and the load resistor kept to a minimum consistent with system power requirements. In the test configuration of Fig. 8 the output rise time is approximately 10ns and the fall time...
PACKAGE DETAILS

Dimensions are shown thus: mm (in).

16-LEAD CERAMIC DIL – DG16

NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

SP8690/SP8691

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